*IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)*
*e-ISSN: 2278-2834,p- ISSN: 2278-8735.Volume 14, Issue 2, Ser. I (Mar.-Apr. 2019), PP 13-18*
*www.iosrjournals.org*

# Design and Analysis of High Performance PISO & PIPOShift Registers

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***Abstract**: Shift registers plays a vital role in many of the digital systems. They are used to store binary information and this binary data can insert or shift using flip flops. By the use of sequential I/O channels shift register plays an important link between systems.With the downscaling of chip size in VLSI technology, the prime factor to design any circuit is power dissipation. This work enumerates implementation of PISO & PIPO shift register by master slave D flip flop as a storage element using BICMOS logic. Cadence EDA tool has used to design proposed shift registers at 180nm technology. Supply voltage is varying between 1.2 to 2v and frequency of clock signal is 200MHz. Results of power dissipation for the proposed shift registers have compared with the results of conventional design using CMOS technology, which clearly shows that proposed circuits have less power dissipation compared to conventional circuits.*

***Keywords:**PISO & PIPO Shift Register, BICMOS, Master-Slave D flip flop,Latch up, Cadence.*

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Date of Submission: 11-03-2019 Date of acceptance: 27-03-2019

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## I. Introduction

An n bit shift register has n flip flops to store n bits of information along with combinational gates to perform data processing tasks which control whenever some new information has transferred into shift register. Flip flops are connected in cascade configuration to form shift register and output of first flip flop is connected to the input of next flip flop and so on. Same clock pulse is given to all the flip flops. As the main motive for any VLSI circuit is to reduce power dissipation, to fulfil these needs many new techniques are introducing by the researchers. Here parallel in serial out (PISO) and parallel in parallel out (PIPO) shift registers have designedby the use of BICMOS logic with cadence EDA tool and calculation of power dissipation has been performed. Performance evaluation has been done by comparing the results of power dissipation for the proposed circuit with the results of conventional design using CMOS technology. BICMOS logic has introduced to get advantages of both BJT and CMOS logic. Because of CMOSlogic power consumption has reduced and due to BJT high speed & high current driving capabilities has introduced in the circuit. Also latch up problem is completely eliminated. [1]

In prior done researchwork, shift register circuit has implemented by using many techniques aiming to reduce power dissipation.

In [1], Divya Bora et.al. designed some digital circuits with BICMOS logicusing Tanner EDA tool to obtain benefits of low static power, large current driving capabilities, high switching speed and high gain. Latch up can be vanished by the use of this logic.In [2], Achyutpandey et. al. used Microwind design and simulation tool to implement 4-bit shift register with self-clocked D flip-flop as a storage element at 90nm technology. The aim of doing this is to reduce power consumption, delay and area of the proposed circuit. Proposed SISO shift register has average power consumption of 107 μw and delay of 257ps. Proposed SIPO shift register has average power consumption of 182μw.Proposed PISO shift register has average power consumption of 155μw. Proposed PIPO shift register has average power consumption of 123μw. In [3], Raj Kumar Mistri et. al. designed a 4-bit Universal shift register using GDI technique & TG. LTspice XVII has used for the purpose of simulation. This paper concludes that GDI technique has less power dissipation and delay compared to TG technique. GDI technique has delay of 46.4μs and power dissipation of 633.8μw for the proposed circuit.

In [4], A.Lakshmi1 et. al. used modified design of D flip flop to implement a 12-bit Parallel In Parallel Out shift register at 180nm technology. The motive behind this is to implement a positive edge triggered conventional D flip flop with high speed and less power consumption. This proposed PIPO shift register has power consumption of 0.028mw. In [5], Saranya.Met. al. implemented a universal shift register with the use of conventional static master slave flip flop at afrequency of 250MHz. This proposed circuit improve power delay product. For the simulation of results H spice tool hasused.In [6], Noor M. Nayeemet. al.designed reversible shift registers (SISO, SIPO, PISO, PIPO) and a universal shift register. These proposed circuits have advantage

of low transistor count, which make it more efficient compared to conventional design.In [7], CH. Jayaprakashet. al. implemented a PIPO shift register using 50nm technology at 1GHz frequency. Analysation of average power, delay and power delay product have done for the proposed shift register circuit.

In this paperPISO & PIPO shift register have been implemented at 180nm technology using BICMOS logic. In section 2 working of proposed shift registercircuit has explained. Section 3showsschematics of shift registers and components using Cadence Virtuoso schematic editor.In section 4 simulation results for all the schematics have shown.Section5 concluded the paper.

## II. Proposed Shift Registers

Shift register has used for the transmission of data just after storing it in serial or parallel mechanism. Serial manner means processing of bits sequentially and parallel manner means processing of bits in parallel. On structural basis shift register hasfour different modes. In Serial-In Serial-Out (SISO) shift register with every clock, there is a shift of one bit either in left or right with serial feed of input data.In Serial-In Parallel-Out (SIPO) shift registeroutput data has stored in parallel and input data feed in serial manner.[9]Parallel-In Serial-Out (PISO)shift register is a type of register in which input data has stored in parallel manner and out in serial manner. In Parallel-In Parallel-Out (PIPO) shift register input loads in parallel manner and also out in parallel manner. In this paper we are implementing two operating modes of shift registers which are PISO & PIPO.The implementation of PISO shift register has shown in Fig.1.

Each flip flop has respective input from D0 to D3. If the control signal Shift/load =0 then each flip flop loaded with input. If the control signal Shift/load =1 then shifting has performed and output has taken from the last flip flop serially. The implementation of PIPO shift register has shown in Fig.2. In this as the input has loaded to each flip flop, instantly output has obtained from each flip flop. Once the clock has given to the flip flops, they generate output simultaneously.

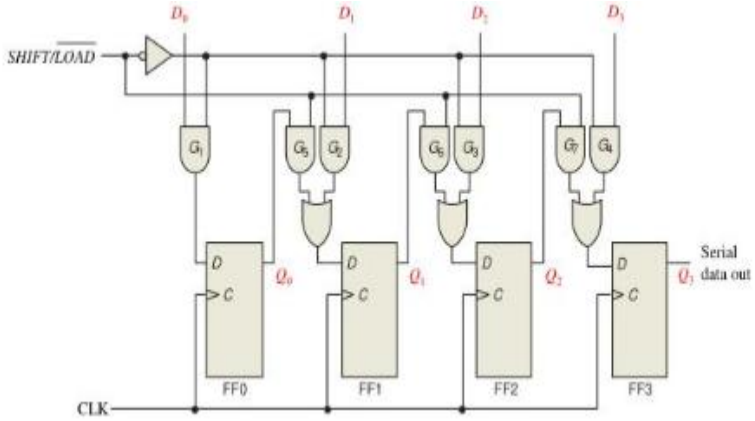


**Figure 1:**Circuit for PISO shift register

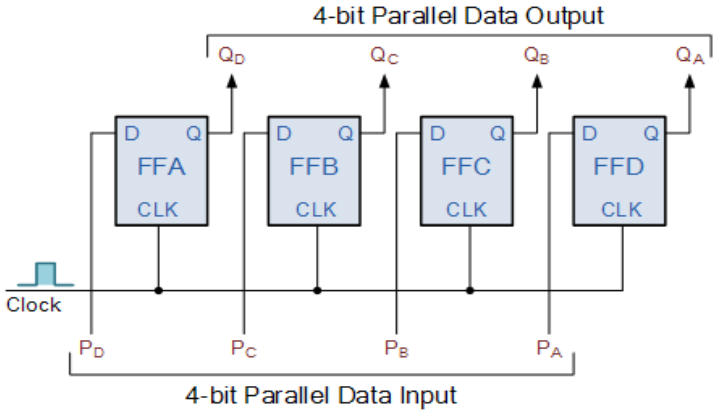


**Figure 2:**Circuit for PIPO shift register

Master-slave D flip flop shown in figure 3. For the function of holding its output, clock inverter is used and we have two signals clock and inverted clock to disable the inputs. There may be possibilities of glitches at the gate node of circuit and to eliminate it PMOS MP3 has used. This circuit results in reduction of delay & area. This circuit never affected because of clock skew.

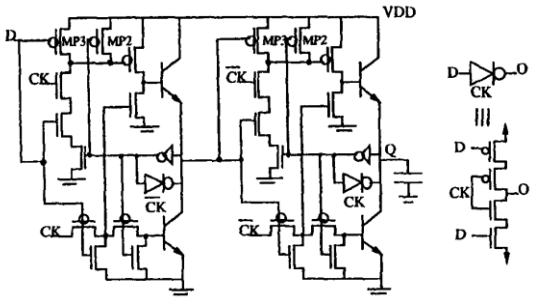


**Figure 3:**Master- Slave D flip flop circuit implementation (using BICMOS logic)

## 1. SCHEMATIC DESIGN

To implement theschematic design for PISO & PIPO shift registers we are required to design all its components independently then implement the circuit for shift registers by using all of them. Cadence Virtuoso schematic editorhas used to design all the schematics using BICMOS logic with below specifications: Length L=180nm, Width W= 2 µm. Figure 4 represents schematic design for inverter. Figure 5 shows schematic design for AND gate. figure 6 shows implementation of XOR gate. Figure 7 &8 showing the schematic design for PISO & PIPO shift registers respectively.

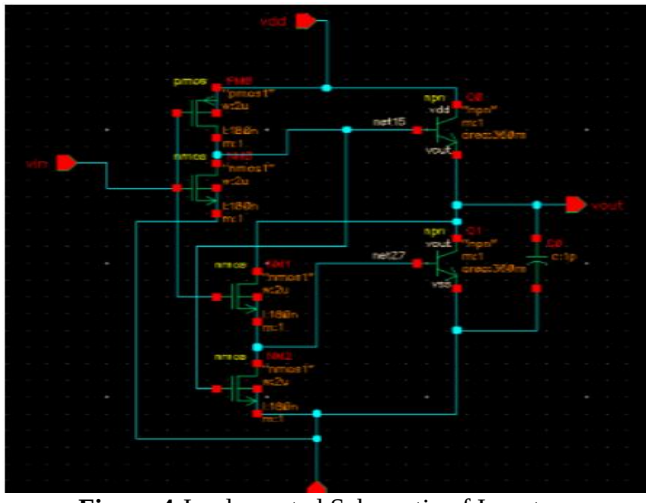

**Figure 4:**Implemented Schematic of Inverter

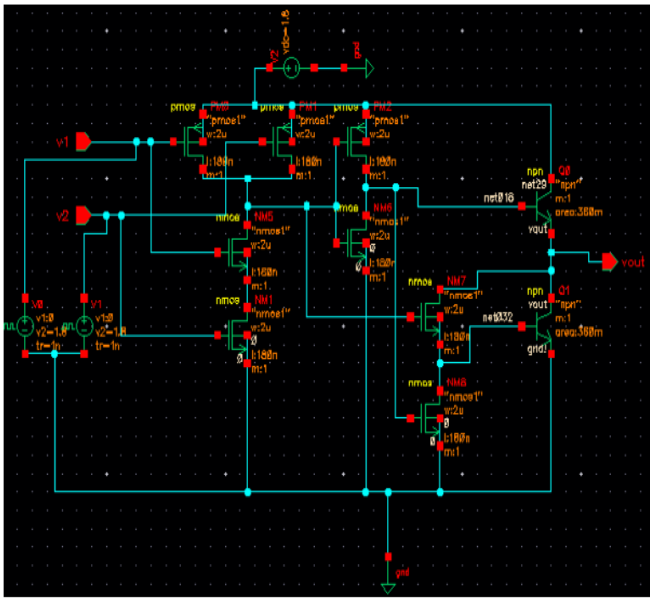

**Figure 5:**Implemented Schematic of AND gate

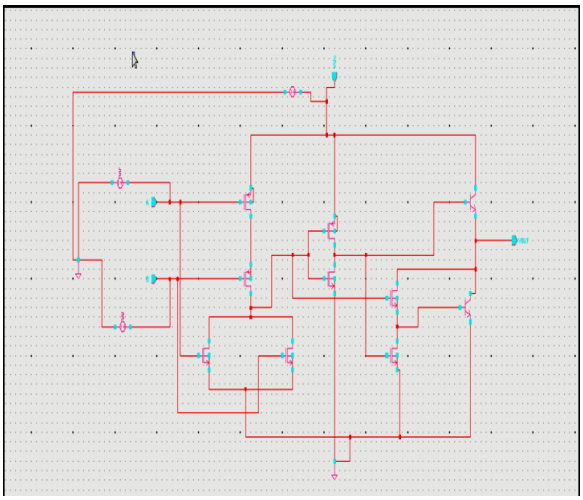

**Figure 6:**Implemented Schematic of OR gate

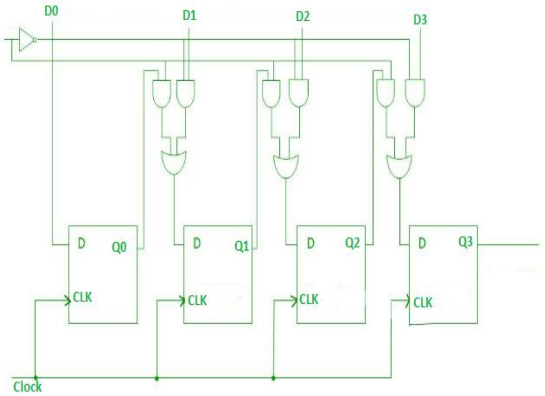


**Figure 7:**Implemented Schematic of PISO shift register

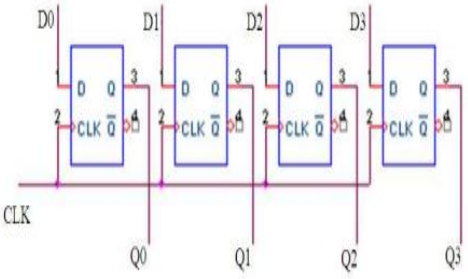


**Figure 8:** Implemented Schematicof PIPO shift register

## 2. SIMULATION RESULTS

Analog simulation method of cadence design environment has used to analyse and verify the proposed design of shift registers on 180nm technology.Supply voltage is varying between 1.2 to 2v and frequency of clock signal is 200MHz. The analysation of performance for the proposed shift register circuits have done by comparing the results of its power dissipationwith the results of conventional design. Table 1 showing the comparison results. Simulation results for not, and, xor gates, PISO & PIPO shift register have shown in following figures.

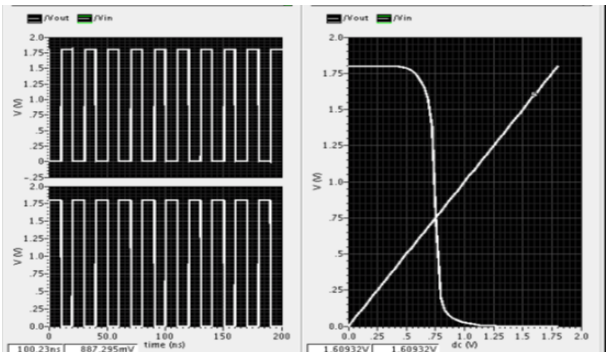

**Figure 9:**Output Waveform of Inverter

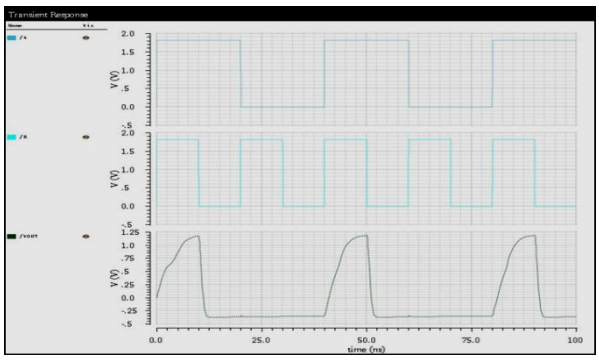

**Figure 10**: Output Waveform of AND gate

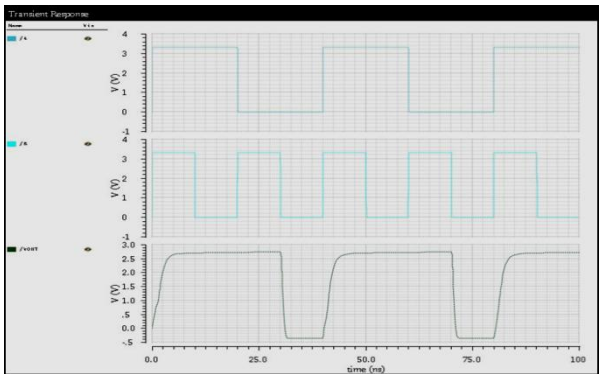

**Figure 11:**Output Waveform of OR gate

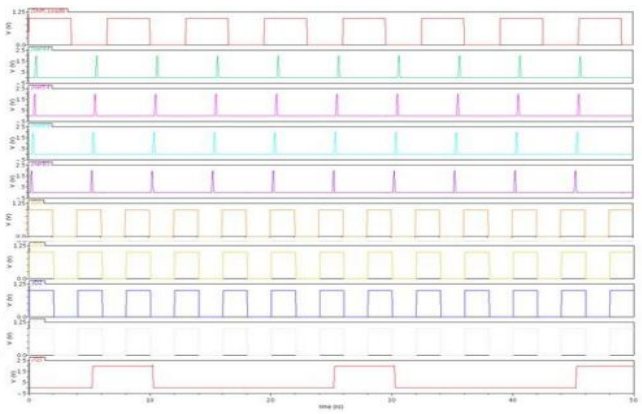

**Figure 12:** Output Waveformof Proposed PISO shift register

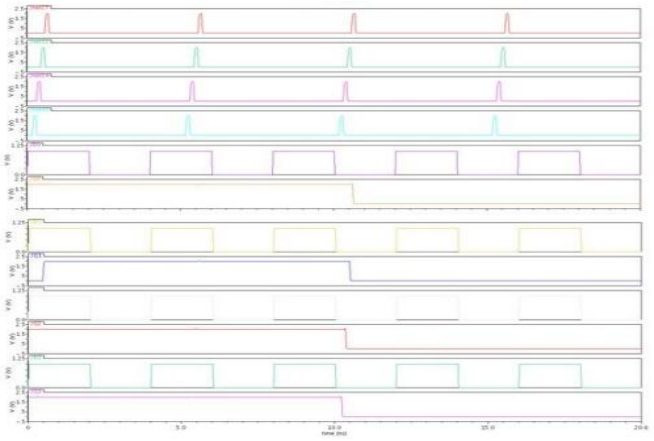

**Figure 13:**Output Waveform of Proposed PIPO shift register

**Table 1:**Table for comparison of Power Dissipation

| Design Technique | Existing design using CMOS logic | Proposed Design using BICMOS logic |
|---|---|---|
| PISO | 0.22m w | 104 µw |
| PIPO | 0.109mw | 120µw |

## III. Conclusion

In this paper master slave D flip flop has used to design 4-bit PISO & PIPO shift register. Proposed shift registers have been implemented by using BICMOS logic and design is simulated in cadence simulation platform using 180nm technology.The aim of doing this is to reduce power dissipation and implement a power efficient shift register that can be use in various complex circuits.By comparing their results with the conventional design we can conclude that proposed shift register has less power dissipation. Comparison results have shown in Table 1. To optimize the design in future improved routing and placement algorithms can be implement.

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